Time to space conversion (TSC) [1] has been implemented for routine use with different types of linear delay line readout detectors in the TSC-1001 module [2], using an ASIC that has the event counters on the chip. An ASIC, which does not contain counters and is thus also suitable for use with area detectors, is also available.

The performance of the TSC-1001 has been characterized in a number of practical applications using, in particular, conventional linear detectors with continuous delay lines. To image the $i$th section of such a delay line the two cathode signals must be delayed by $(i-1)N$ and $T-(i-1)N$ respectively, where $T$ is the total delay of the line and $N$ the transit delay of the ASICs. The DL-1001 stand-alone NIM delay module, which was built for this purpose, provides 16 channels with individual or common inputs. The delay of the output signal of each channel (30 – 350 ns) is set by dipswitches. An alternative using fan out modules and hardwired LC-delay lines was also investigated. One of the advantages of TSC with continuous delay lines lies in the reduced conversion time, which is partly due to the fact that no additional delay is required to order the start and stop signals of the cathode. Moreover, rejection of uncorrelated events is fully guaranteed, in contrast with conventional time to digital converters.

TSC was also successfully tested for the readout of small groups of wires in multianode (wire per wire) detectors. This promises to considerably simplify the readout electronics of such detectors with a minimum loss in performance compared to full parallel readout. The method thus presents a universal solution to delay line readout of linear detectors using continuous or segmented lines or multianode detectors.

The results of tests with the second ASIC, which forms the basis of another stand-alone NIM module, the TSC-1002, will also be illustrated. Readout of area detectors is possible using two such modules in a master-slave configuration.

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**References**


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